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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,556	JACOB, ROJIT	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10,19,20,27-35,39-48 are rejected under 35 U.S.C. 102(b) as being anticipated by Winegarden (patent No. 6,467,009).

3. Winegarden taught the invention as claimed including a data processing ("DP") system comprising (as per claims 1,19,27,33,40,41,42,47):

a) First semiconductor device having a plurality of computation nodes (e.g., see fig. 18,21 col. 3, lines 43-49, and col. 36, lines 52-67);

b) Second semiconductor device having a microprocessor-based node adapted to function as a system controller and a plurality of computation nodes e.g., see figs.10,49 and col. 3, lines 43-65 and col. 36, lines 52-67)

c) Bus for inter-connecting the first semiconductor device to a second semiconductor device in a ring topology whereby the microprocessor-based node allocates a plurality of operations among said computation nodes of the first and second semiconductor devices over the interconnecting bus and receives the results of the operations over the inter-connecting bus (e.g., see fig. 10, 40 and col. 36, line 45-col. 37, line 45)[after completion is signaled by the slave device the master device can generate a read or write transaction to the slave chip accessing results].

4. As per claim 2, Winegarden taught the computation nodes on the first and second semiconductor devices include at least one of the following node types: arithmetic , bit manipulation node , reduced instruction set node and finite machine node (e.g., see col. 34, lines 4-49).

5. As per claim 3,34,35,42,45 Winegarden taught the digital system includes a plurality of nodes of which can perform at least one type of operation and wherein the microprocessor allocates functions temporally and spatially among nodes of the first and second devices (eg., see figs. 10, 18,19 and col. 36, line 45-col. 37, line 44 and col. 19, lines 1-col. 212, line 51).

6. As per claim 4, Winegarden taught a remote processor a bus for interfacing the first and second semiconductor device to the remote processor (e.g. see fig. 42).

7. As per claim 5,28,29 Winegarden taught real-time data source; and third bus interfacing the second semiconductor to the real-time generator (tester debugger is real-time source in figs. 42,37).

8. As per claim 6,31 Winegarden taught a plurality of logic elements (e.g., see figs. 18,19,20,21), each loosely proximate to a corresponding output pad of the first semiconductor device, for sending data and control signals ,a plurality of logic elements (e.g., see figs. 18,19,20,21) each closely proximate to a corresponding input pad of the second semiconductor device, for receiving the data and control signals and means synchronously transferring data and control signals by clocking the logic elements of the first and second semiconductor devices (e.g., see col. 18, line 43-col. 20, line12 and col. 38, lines 21-56 and col. 30, lines 39-67).

9. As per claim 7, 8,9 ,19, Winegarden taught a first core logic clock provided to each of said nodes of the first semiconductor device; a second core logic clock provided to each of the nodes of the second semiconductor device, the first and second logic clocks having substantially the same frequency and phase; a first core clock for clocking logic elements of the first semiconductor device at a selected rate where the first bus clock is derived from the first core logic clock a second clock for clocking the logic elements of the second semiconductor device at the selected rate where the second bus clock is derived from the second core logic clock and synchronizing signal generated by the first semiconductor device (e.g., see col. 30, lines 38-67 and col. 37, lines 10-15 and col. 33, lines 28-49). And signal for indicating valid data and control signals to the second semiconductor device (e.g., see col. 37, lines 23-35)[the completion signal indicates that the slave device is completed processing and therefore the data is valid and can be accessed by master device].

10. As to claim 10,30 Winegarden taught the first and second semiconductor devices are coupled in a ring with the inter connecting bus coupled a output port of the first semiconductor device to an input port of the second semiconductor device and further coupling an output port of the second semiconductor device to an output port of the second semiconductor device to an input of the first semiconductor device (e.g., see figs.40,41).

11. Further as per claim 19,31 Winegarden taught the output port comprises D type flip flops coupled to the corresponding plurality of D type flop flops at the input port (e.g., see figs. 10,11,12).

12. As to claim 20,Winegarden taught coupling up to four computing engines in a ring topology (e.g., see figs., 3, 40).

13. As to claim 27 Winegarden taught a user interface (4220) (e.g., see fig. 42).

14. As to the limitations of claim 32, Winegarden taught one of the plurality of node is a master node that programs the other node (e.g., see fig.41).

15. As to the further limitation of claim 33,39, Winegarten taught the an array of nodes that can perform arithmetic, bit manipulation or finite state function or input/ output (e.g., see fig. 18, 19, when programmed by the master module.

16. As to claim 43, Winegarden taught means to access core processor and memory debug error conditions e.g,. see co. 37, line 46-col. 38,line 20).

17. As to claim 44 Winegarden taught means for handling node to node communications (e.g., see fig. 22).

18. As per claim 46, Winegarden taught means for controlling initiation of operation of computation elelement upon reset or power on (e.g., see co 35,lines 54-67) and col. 36, lines 49-67).

19. As to the cache limitation of claims 47,48, Winegarten taught an SRAM memory (e.g., see fig.42)

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 11-13,14-18,21-26,36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winegarden (patent No. 6,407,009).

22. As per claim 11,12,21,22,24 Winegarden taught a system where identical modules can each perform as a master or slave and plural of these modules can be connected for performing operations in a master/slave manner (eg., see col. 36, line44-col. 37 , line 35 and col.3 line42-col. 4 line 55) (e.g.,see fig. 37). In order to allow the plural master processors to operate and to share the slave processors to keep the slave processors performing the optimum amount of processing one of ordinary skill would have been motivated to send signals between master devices destined to a slave device wherein the master device would have a had to determine the destination for the data or code and then transfer the data packet to the destination.

23. As per claim 14 Winegarden taught a) First semiconductor device having a plurality of computation nodes (e.g., see fig. 18,21 col. 3, lines 43-49, and col. 36, lines 52-67); b) Second semiconductor device having a microprocessor-based node adapted to function as a system controller and a plurality of computation nodes e.g., see figs.10,49 and col. 3, lines 43-65 and col. 36, lines 52-67) Bus for inter-connecting the first semiconductor device to a second semiconductor device in a ring topology whereby the microprocessor-based node allocates a plurality of operations among said computation nodes of the first and second semiconductor devices over the interconnecting bus and receives the results of the operations over the inter-connecting bus (e.g., see fig. 10, 40 and col. 36, line 45-col. 37, line 45)[after completion is signaled

by the slave device the master device can generate a read or write transaction to the slave chip accessing results].

24. As to the limitations of claim 13,14,15,23 Winegarden taught master chip and directly connected slave chip receiving chip enable signals. In the situation where the data was written to a master or slave that was not directly connected one bit chip enable would not provide the identification of the chip. Therefore one of ordinary skill would have been motivated to send a device ID of the source or destination to ensure the data was sent to the proper destination. Also when an error in the device Id was made one of ordinary skill would have motivated to discard the packet (e.g., see fig. 37). Further to the "adapted for" language this language does not definitely claims the corresponding limitation and therefore the corresponding limitation following "adapted for" is given no weight.

25. As to claim 16,17 Windegarden taught each of the computing engines includes an output port coupled to an input port of the next adjacent adaptive computing engine (e.g., see figs. 3) comprising two three or four computing engines.

26. As per claim 18, Winegarden taught the output port comprises D type flip flops coupled to the corresponding plurality of D type flop flops at the input port (e.g., see figs. 10,11,12).

27. As per claim 25,26 Winegarden taught a FIFO buffer 1440) for data transferred between modules (e.g., see fig. 14)

28. As per claim 26 Winegarden taught a signal for indicating valid data and control signals to the second semiconductor device (e.g., see col. 37, lines 23-35)[the completion signal indicates that the slave device is completed processing and therefore the data is valid and can be accessed by master device].

29. As per claims 36, 37,Winegarden taught interfacing the system with a workstation (e.g., see fig. 42) therefore it would have been within the level of skill of one of ordinary skill to download executable code from the internet (including operating system code) for use by the first processing node. Due to the ability to access vast amounts of data or code one of ordinary skill would have been motivated to use the Internet to download the data.

30. As per claim 38, Winegarden taught the digital system includes a plurality of nodes of which can perform at least one type of operation and wherein the microprocessor allocates functions temporally and spatially among nodes of the first and second devices (e.g., see figs. 10, 18,19 and col. 36, line 45-col. 37, line 44 and col. 19, lines 1-col. 212, line 51).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hudson (patent No. 6,134,605) disclosed a redefinable signal processing subsystem (e.g. see abstract).

Dowling (patent No. 6,760,833) disclosed a split embedded DRAM processor (e.g., see abstract).

Zemlyak (patent No. 6,604, 189) disclosed a master slave processor (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER